above the channel;

a control gate formed adjacent to and insulated from the floating gate; and

an insulative layer of amorphous carburized silicon [formed] grown on the channel and located between the channel and the floating gate.

4. [Twice Amended] An integrated circuit capacitor supported by a semiconductor substrate, the capacitor comprising:

a first conductor layer supported by [the] a semiconductor substrate;

a dielectric layer of amorphous carburized silicon [formed] grown on top of the first conductor layer; and

a second conductor layer formed on top of the dielectric layer.

5. [Amended] The capacitor of claim 4 wherein at least part of the layers extend substantially vertically from a general surface of the substrate and the amorphous carburized silicon was grown on the first conductor layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

20. [Amended] A memory cell comprising:

a floating gate; and

a layer of amorphous carburized silicon grown on a substrate and located between the floating gate and [a] the substrate.

21. [Amended] The memory cell of claim 20, further comprising:

a source region in the substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region, the channel region being separated from the floating gate by the layer of amorphous carburized silicon; [and]

a control gate separated from the floating gate[.]; and

wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

24. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate; and

a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

29. [Amended] A semiconductor device comprising:

a first conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown over the first conductive layer; and

a second conductive layer over the layer of amorphous carburized silicon.

31. [Amended] The semiconductor device of claim 29 wherein:

the first conductive layer comprises polysilicon; [and]

the second conductive layer comprises polysilicon[.]; and

the layer of amorphous carburized silicon was grown over the first conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

32. [Amended] A memory cell comprising:

a first conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown over the first conductive layer; and

a second conductive layer over the layer of amorphous carburized silicon.

35. [Amended] The memory cell of claim 32 wherein:

the first conductive layer comprises polysilicon; [and]

the second conductive layer comprises polysilicon[.]; and

the layer of amorphous carburized silicon was grown over the first conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

36. [Amended] A capacitor comprising:

a first conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown over the first conductive layer; and

a second conductive layer over the layer of amorphous carburized silicon.

38. [Twice Amended] The capacitor of claim 36 wherein:

the first conductive layer comprises polysilicon; [and]

the second conductive layer comprises polysilicon[.]; and

the layer of amorphous carburized silicon was grown over the first conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

39. [Amended] The integrated circuit field effect transistor of claim 1, further comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region; [and]

a gate isolated from the channel region by the gate insulator[.]; and

wherein the gate insulator was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

40. [Amended] The integrated circuit field effect transistor of claim 1, further comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate isolated from the channel region by the gate insulator; [and]

a polysilicon control gate separated from the floating gate by a layer of insulating material[.]; and

wherein the gate insulator was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

41. [Amended] The integrated circuit field effect transistor of claim 2 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate; [and]

the channel comprises a channel region in the substrate between the source region and the drain region[.]; and

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

42. [Amended] The integrated circuit field effect transistor of claim 2 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region;

the gate comprises a floating gate isolated from the channel region by the amorphous layer of carburized silicon; [and]

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

43. [Amended] The device of claim 3 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region; [and]

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material[.]; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

44. [Amended] The transistor of claim 24 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate; [and]

the drain region comprises an n+-type drain region in the substrate[.]; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

45. [Amended] A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

46. [Amended] A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region between the source region and the drain region in the substrate; and

a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

47. [Amended] The transistor of claim 46 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate; [and]

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

48. [Amended] A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region between the source region and the drain region in the substrate;

a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate; and

a polysilicon control gate separated from the floating gate by a layer of insulating material.

50. [Amended] A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate;

a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region [in the substrate]; and

a control gate separated from the floating gate.

51. [Amended] The memory cell of claim 50 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate; [and]

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material[.]; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

52. [Amended] A memory cell comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate;

a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region [in the substrate]; and

a polysilicon control gate separated from the floating gate by a layer of insulating material.

53. [Amended] A semiconductor device comprising:

a conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the conductive layer; and

a polysilicon layer in contact with the layer of amorphous carburized silicon.

54. [Amended] The semiconductor device of claim 53 wherein:

the conductive layer comprises polysilicon; [and]

the layer of amorphous carburized silicon was grown on the conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

the semiconductor device further comprises a source/drain diffusion in the substrate.

55. [Amended] A semiconductor device comprising:

a first polysilicon layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the first polysilicon layer; and

a second polysilicon layer in contact with the layer of amorphous carburized silicon.

56. [Amended] The semiconductor device of claim 55, further comprising:

a source/drain diffusion in the substrate[.]; and

wherein the layer of amorphous carburized silicon was grown on the first polysilicon layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

57. [Amended] A memory cell comprising:

a conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the conductive layer; and

a polysilicon layer in contact with the layer of amorphous carburized silicon.

58. [Amended] The memory cell of claim 57 wherein:

the conductive layer comprises polysilicon; [and]

the memory cell further comprises a source/drain diffusion in the substrate[.]; and

the layer of amorphous carburized silicon was grown on the conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

59. [Amended] A memory cell comprising:

a first polysilicon layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the first polysilicon layer; and

a second polysilicon layer in contact with the layer of amorphous carburized silicon.

60. [Amended] The memory cell of claim 59, further comprising:

a source/drain diffusion in the substrate[.]; and

wherein the layer of amorphous carburized silicon was grown on the first polysilicon layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

61. [Amended] A capacitor comprising:

a conductive layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the conductive layer; and

a polysilicon layer in contact with the layer of amorphous carburized silicon.

62. [Amended] The capacitor of claim 61 wherein:

the conductive layer comprises polysilicon; [and]

the capacitor further comprises a source/drain diffusion in the substrate[.]; and

wherein the layer of amorphous carburized silicon was grown on the conductive layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

63. [Amended] A capacitor comprising:

a first polysilicon layer supported by a substrate;

a layer of amorphous carburized silicon grown on [in contact with] the first polysilicon layer; and

a second polysilicon layer in contact with the layer of amorphous carburized silicon.

64. [Amended] The capacitor of claim 63, further comprising:

a source/drain diffusion in the substrate[.]; and

wherein the layer of amorphous carburized silicon was grown on the first polysilicon layer in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

Please add the following new claims:

65. [New] The transistor of claim 45 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

66. [New] The transistor of claim 48 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.